Amendments to the Specification:

Please replace paragraph **[020]** with the following amended paragraph:

The arbitration control circuit 210 is further coupled to the high-speed link 134 to receive arbitration packets from downstream memory hubs. As will be explained in more detail below, arbitration packets are provided in advance of an associated memory response, and provide the arbitration control circuit 210 of an upstream memory hub with information to enable the appropriate path through the receiving memory hub in anticipation of receiving the associated memory response. Additionally, the arbitration control circuit 210 generates an arbitration packet to be provided prior to an associated LMR to serve as an early indication of the associated memory response when data is read from the memory devices 148 (Figure 1) in response to a read request. As previously discussed, the arbitration packet will provide upstream memory hubs with appropriate information and give the respective arbitration control circuits 210 time to make decisions regarding enablement of the appropriate data paths before the memory response arrives. The arbitration control circuit 210 prepares the arbitration packet while read data for the memory response is being retrieved from memory devices 148. The arbitration packet is provided through a switch 212 to either the multiplexer 208 or the local response queue 202, depending on whether if the upstream memory hub is idle or busy. The multiplexer 208, under the control of the arbitration control circuit, couples the high-speed link 134 to receive memory responses from the remote response queue 206 or the bypass path 204, arbitration packets from the arbitration control circuit 210, or arbitration packets and memory responses from the local response queue 202. ~~For example, the number and type of data fields of the data structure 300 can be changed or the number of bits for each bit time can be changed and still remain within the scope of the present invention.~~ In an alternative embodiment of the present invention, the arbitration packets are generated in an arbitration packet circuit, rather than in the arbitration control circuit 210, as shown in Figure 2. Additionally, although shown in Figure 2 as providing the arbitration packet to the multiplexer 208 to be injected into the stream of data, the arbitration packet can alternatively be provided to the local response queue 202 and placed before the associated read response packet to be injected into the data stream. It will be appreciated by those ordinarily skilled in the art that modifications to the embodiments of the

present invention, such as the location at which the arbitration packet is generated or the manner in which the arbitration packet is placed into the data stream prior to the associated read packet, can be made without departing from the scope of the present invention.

Please replace paragraph **[021]** with the following amended paragraph:

Figure 3 illustrates a data structure 300 for arbitration packets and memory responses according to an embodiment of the present invention. The data structure 300 is divided into 8-bit bytes of information, with each byte of information corresponding to a sequential bit-time. Each bit-time represents an increment of time in which new data can be provided. A response header field 302 includes two bytes of data that indicate the response is either an arbitration packet or a memory response. An address field 304 includes data that is used to identify the particular hub to which the arbitration packet or memory response is directed. A command code field 306 will have a value to identify the data structure 300 as an arbitration packet, and not as a memory response. Arbitration packets and memory responses are similar, except that the data payload of data fields 308 are "don't cares" for arbitration packets. In the data structure 300, all 16 bits of size fields 310 carry the same value to indicate the size of the data payload carried by the memory response. For example, a "0" indicates that 32 bytes of data are included, and a "1" indicates that 64 bytes of data are included. It will be appreciated by one ordinarily skilled in the art that the embodiment of the data structure 300 shown in Figure 3 has been provided by way of example, and that modifications to the data structure 300 can be made without deviating from the scope of the present invention. For example, the number and type of data fields of the data structure 300 can be changed or the number of bits for each bit time can be changed and still remain within the scope of the present invention.